CLAIMS:

1. A semiconductor device comprising:

a semiconductor substrate;

a first insulating film formed over said semiconductor substrate;

a capacitor formed over said first insulating film, and having one electrode which includes an extension extending over said first insulating film;

a second insulating film formed over said first insulating film;

a contact hole formed through said second insulating film and said extension of the one electrode; and

a conductor pattern burying said contact hole.

2. A semiconductor device comprising:

a semiconductor substrate;

a first insulating film formed over said semiconductor substrate;

a conducting plug formed in said first insulating film;

a storage electrode formed over said first insulating film, and electrically connected to said conducting plug;

a capacitor dielectric film formed over said storage electrode;

an opposing electrode formed over said capacitor dielectric film, and having an extension extending over said first insulating film;

a second insulating film formed over said opposing electrode;

a contact hole formed through said second insulating film and said extension of the opposing electrode; and

a conductor pattern burying said contact hole.

3. A semiconductor memory device comprising:

a semiconductor substrate;

a switching transistor including an insulated gate formed on the substrate and source/drain regions formed in the substrate on both sides of the insulated gate;

an insulator laminate formed on the substrate, and including a lower part covering said insulated gate and a higher part formed over the lower part;

a first conductive plug formed through the lower part of the insulator laminate and connected to one of the source/drain regions;

a storage electrode formed in the higher part of the insulating laminate and electrically connected to the first conducting plug;

a capacitor dielectric layer formed on the storage electrode;

an opposing electrode covering the capacitor dielectric layer and having an extension formed over the lower part of the insulator laminate;

a lower conducting member formed within the lower part of the insulator laminate;

a second conductive plug formed through the higher part of the insulating laminate and the extension of the opposing electrode and electrically connected to the opposing electrode at a side surface;

a third conductive plug formed through the insulator laminate above said lower conductive member, and electrically connected to an upper surface of the lower conductive member.

4. The semiconductor memory device according to claim 3, wherein said lower part of the insulator laminate includes a silicon nitride layer at an uppermost level.

5. The semiconductor memory device according to claim 4, wherein said silicon nitride layer is patterned after the opposing electrode.

6. The semiconductor memory device according to claim 3, wherein said storage electrode has a cylinder shape.

7. The semiconductor memory device according to claim 6, wherein said storage electrode is formed of a silicon layer.

8. The semiconductor memory device according to claim 3, wherein said higher part of the insulator laminate has a planarized upper surface.

9. The semiconductor memory device according to claim 8, wherein said second and third plugs are contiguous to wiring pattern formed over the higher part of the insulator laminate.

10. The semiconductor memory device according to claim 3, wherein said opposing electrode is formed of a silicon layer.

11. The semiconductor memory device according to claim 10, wherein said lower part of the insulator laminate includes a silicon nitride layer at an uppermost level, which is patterned after the opposing electrode.

12. The semiconductor memory device according to claim 10, wherein said lower conducting member includes a metal silicide layer at its top level.

13. The semiconductor memory device according to claim 3, further comprising a fourth conducting plug formed through the insulator laminate and reaching the semiconductor substrate.

14. The semiconductor memory device according to claim 12, wherein said lower conducting member has oxide side walls and a silicon nitride layer

covering the metal silicide layer and the oxide side walls.

15. The semiconductor memory device according to claim 3, wherein said insulated gate comprises a gate insulating layer formed on the semiconductor substrate, a gate silicon layer formed on the gate insulating layer, a gate silicide layer formed on the gate silicon layer, oxide side walls formed on side surfaces of the gate silicon layer and the gate silicide layer, and a gate silicon nitride layer covering the gate silicon layer and the oxide side walls.

16. The semiconductor memory device according to claim 15, wherein said first conducting plug is contiguous to the gate silicon nitride layer.

17. The semiconductor memory device according to claim 3, further comprising :

a fifth conducting plug formed through the lower part of said insulator laminate and connected to another of said source/drain regions; and

a bit line formed over the lower part of and in the higher part of said insulator laminate and connected to said fifth conducting plug.

18. The semiconductor memory device according to claim 17, wherein said bit line includes a conducting bit layer, oxide side walls on side walls of the conducting bit layer, and a bit silicon nitride layer covering the conducting bit layer and the bit silicon nitride layer.

19. The semiconductor memory device according to claim 18, wherein said storage electrode is contiguous to said bit silicon nitride layer.

20. The semiconductor memory device according to claim 18, wherein

said conducting bit layer includes a silicon bit layer and a silicide bit layer formed on the silicon bit layer.

21. The semiconductor memory device according to claim 18, further comprising:

a medium conducting member formed over the lower part of and in the higher part of said insulator laminate.

22. The semiconductor memory device according to claim 21, wherein said medium conducting member comprises a common structure as said bit line.

23. The semiconductor memory device according to claim 22, further comprising a sixth conducting plug formed through the higher part of said insulator laminate and the silicon nitride layer of the medium conducting member, and connected to the silicide layer of the medium conducting member.